Evaluation of the Doctoral Thesis

"Digital Circuits Testing
Based on Pattern Overlapping and Broadcasting"

by Ing. Martin Chloupek
submitted to Czech Technical University in Prague

1. Research Area and Challenges
Test technology for integrated circuits and systems is essential for the quality and the dependability of electronic systems. Therefore it has been a field of intense research since about the late 1970s. Over decades, test has been the essential bottleneck in IC production, since testing costs threatened to dominate the overall costs for IC manufacturing. In particular, the exploding volume of test data, both for test inputs and for test outputs, had to be confined by innovative techniques for test data compression. The other alternative, already developed in the 1980s, was built-in self test (logic BIST). Innovative techniques for test input data compression in combination with structured design for testability by scan-test have been developed since about the late 1990s. Commercial tools that combine test pattern generation, off-line test compression and on-line on-chip test de-compression, became commercially available from EDA-vendors such as Mentor Graphics by about 2006. They are now part of every commercial system for digital IC design. Still this area cannot really be considered as “done” for several reasons. First, any significant progress in test data compression or test application time makes sense, since it directly reduces the cost of testing. Second, extra hardware that needs to be implemented for test support can become faulty itself and harm the production yield. Therefore schemes that deliver good compression results at a minimum cost in extra hardware are attractive. Third, compaction schemes so far address mainly static faults, while testing also for dynamic faults such as transition faults with a minimum extra overhead in cost and power makes the next challenge. In this thesis, the author has a focus only on test input compaction for static faults. This puts him into direct competition with developments at major EDA companies. Unfortunately, the thesis does not address the even more challenging problem of test output data compression.

2. Structure and Content of the Thesis
At the beginning of the thesis we find a comprehensive table of contents and lists of figures, tables and abbreviations.
The first chapter is a relatively short introduction which describes the motivation for the work done, the main contributions, and the structure of the thesis.
The second chapter is entitled “background and state-of-the-art”. The basic principle of IC test set-ups is shortly described. Self test is not addressed. The next sub-chapter entitled “fault models” makes a distinction only between permanent faults and temporary faults. It is true that IC production test can address only permanent faults. The main fault model to describe static faults is the “single stuck-at fault” (SSA) model. It certainly has the widest practical acceptance. However, dynamic faults such as transition faults and delay faults have been dealt with also since the 1980s, and since about 2000 also methods of testing such faults based on scan-test structures has been a point of intense research. This point is not addressed in the thesis. Mutual masking of several stuck-at faults is also a matter of recent research not addressed here. Therefore the thesis is based on the assumption of single stuck-at faults, whereby the vast majority of multiple stack-at fault conditions is also covered implicitly.
The next sub-chapters deal with testing combinational logic and test pattern generation. The basic methods described are valid for single stuck-at faults in combinational logic. As for the ATPG process described, it is basically correct, but it might have been mentioned that a typical ATPG process will not directly produce a minimum-size test set on one hand and that produced test vectors from deterministic ATPG typically contain a number of bits that need not be set deterministically for the targeted fault. However, if such bits are randomly filled as previously done in industrial ATPG processes, resulting test vectors will often "catch" hard-to-test faults just by chance. As mentioned in the next sub-chapter, test generation for sequential circuits is extremely difficult at best. But many of today's commercial ATPG tools do have a limited capability for sequential ATPG, if they support testing for transition faults via scan-path structures using local feedbacks to create the second test vector in a pair. As described here shortly, scan test technology is the actual core of structured design for testability. While standard scan-test seems to be the dominating technique, there are extended scan techniques such as "double latched scan" or "broadside test", which can also support testing for dynamic faults. Next schemes of test data minimization are introduced, starting with built-in self test (BIST). It is not mentioned here that BIST typically also involves test output data compaction in time by e. g. multi-input signature registers. Such techniques may be applicable also in combination with test-input data compaction techniques, but there has to be a mutual coordination. At this point, the author also introduces the basic architecture of multiple parallel scan chains that are fed in parallel from a linear feedback shift register. Multiple parallel scan chains become a must due to the extremely high number of combinational "pseudo"-inputs in today's designs such as "Systems on Chip" (SoCs), since a single scan chain would take far too much time to fill. This is the basic architecture both for BIST (STUMPS) as well as for several techniques of test data input compression. Test data compression comes next, whereby specific techniques of linear compression / de-compression are described more in detail. They use LFSRs, ring oscillators, or XOR-based phase shifters for de-compaction. Techniques that use pseudo-random sequences from LFSRs that can deterministically be modified, e. g. by re-seeding, are also mentioned. The author is right in his perception that most such techniques require specific adaptations and even successive coding in the ATPG-process itself. Hence any user of such a commercial technology will depend on specific ATPG tools. Independence from a specific ATPG tool is actually one of the essential highlights of the compaction technology developed in this thesis.

The concept of pattern broadcasting by feeding several parallel scan chains is explained next, also referencing the "Illinois scan" architecture. Pattern overlapping, which is elaborated next, is a vital method for test pattern compaction. However, merging several patterns that are supposed to test independent faults will always minimize the number of "X" (don't care) positions in a single pattern and will hence reduce the chances to compress test input data. For example, a test set that has undergone an overlapping procedure before will hardly allow for a compaction factor of 100 or more, which some EDA companies claim to achieve. Sub-chapter 2.2 describes known methods for test input compaction developed by the major EDA companies. Again the vital problem of test output data compression is not even mentioned.

Sub-chapter 2.2.5 has a focus on previous work done by the group of Prof. Novak at TU Liberec in the area of test input data compression, using both overlapping and de-compaction by multiple scan chains (RESPIN, U. Stuttgart). The final discussion is essentially correct. However, the author does not mention that information on "X" output bits, which need to be masked for output compaction, may actually become a large part of the input data.

The third chapter describes the approach to test input compaction followed by the author in detail. The basic idea is to start with pattern folding and then pattern broadcasting. This is a basic approach not known from industrial EDA tools. The basic hardware structure shown in fig. 3.1 is relatively simple, compared with, for example, Mentor's EDT. However, it imposes a few critical constraints. The scan chains must form, in terms of number and length, a square. With, for example, 1000 scan chains of about 100 bit length each, this is not always compliant with industrial practice. Furthermore, other author avoids such lengthy shift registers and create outputs for extra scan chains by XOR-based "phase shifters". The key issue seems to be that shift in parallel scan chains can
be stalled upon demand for de-coupling patterns. Furthermore, in any rotating pattern, feedback
patterns could be replaced by input patterns. However, this would require a specific control and
specific information from the ATPG process, which also has to be formalized and transferred.

The algorithm introduced to combine similar patterns as effectively as possibly is new and creative.
The weak point is that it needs to allocate specific input bits of the device under test to a specific
scan chain. This is difficult at the level of logic design, because the detailed structure of the scan
chain is often chosen based on neighborhood relations in the layout. As correctly annotated by the
author, this first set of optimization considers only the number and the distribution of “X”-bits in a
test vector, but not conflicting “care” bits. This requires a second step of optimization. Then the
author shows a program flow which combines these steps into a single procedure. The following
table shows results obtained versus previous work done by the same group. Results are clearly visible
and impressive. They also show that there is a clear trade-off between test data volume and test
application time. The necessary hardware overhead is discussed next (figure 3.7). This scheme also
shows a MISR device, apparently to be used for test output compaction. Such compaction, however,
can only work if the scan chains will not produce any “X” (undefined / unknown) outputs, otherwise
there must be a mechanism for “X”-blanking, which is quite expensive in terms of extra input
information. The scheme does not explain how information on selective “stall” of clocks for specific
scan chains is handled. Figure 3.8 shows a surprisingly high overhead specifically for the test
controller indicated in fig. 3., but not described in detail. Tables 3.5 and 3.6 show both hardware
overhead and compression results in comparison with a commercial tool. Readers can only guess
which commercial tool this may have been. The method proposed compares favorably with results
from the commercial tool in terms on hardware overhead and test clock cycles, but it shows very
substantial savings in terms of memory space required on the tester device.

The fourth chapter is entitled “conclusions” and gives a summary and an outlook.
The author compares his results favorably with data from previous work on compaction by the same
group. Essentially, the author claims a reduction in test application time by a factor of 49 with an
increase of test input data by a factor of 8. Tables at the end of the preceding chapter show relatively
good performance at about the level of a commercial tool with substantial savings of storage space
on the tester. Finally, scientific contributions and summarized, and suggestions for future research
are made. Unfortunately, also here the author does not address the need for input information that
can control the X-blanking of outputs. The necessary information needed for that purpose, which
commercial tools need to consider, can reduce the achievable compression rates on real-life circuits
substantially. Finally, there is a list of references and a list of publications, to which the author
contributed, including also citations of his work.

3. Merits and Shortcomings
It must be mentioned that the candidate has worked on an area, which is already covered by all
major companies in the field of electronic design automation (EDA). This means that he had to come
up with at least comparable results in direct competition against teams in these companies that may
be counted by dozens of people. Furthermore, he seemed to have only limited access to commercial
tools and no access to multi-million gate netlists that are typical for industrial “systems on chip”.
The approach taken by the candidate differs significantly from methods known from commercial
tools. It shows significant improvements versus the state-of-the-art in 2 aspects. First, the demand
for test space on the test machine is significantly lower. Second, his method is independent from a
specific tool for automatic test pattern generation.
The weak point is that he does not consider problems of test output compaction, which have, by the
X-output problem, strong implications on the size of test input information as well. Since the
available benchmark circuits may all produce no X-outputs, this may be an excuse.
The thesis is extremely compact with all information on the author’s own work and results allocated
in the third chapter. Essentially, it has the size of a normal Bachelor’s thesis. It is not clear how
information on clock blanking for scan chains is produced, stored, transmitted, and applied.
However, a significant contribution in a narrow field is clearly visible.
It can be stated that the author has given a substantial contribution to the state-of-the-art in his field, documented by a number of international publications and citations by other authors. Therefore the doctoral graduation process can and should be continued.

The author of the dissertation proved the ability to conduct research and achieve scientific results. In accordance with par. 47, letter (4) of the Law Nr. 137/2016 (The Higher Education Act) I do recommend the thesis for the presentation and defense with the aim of receiving the Ph.D. degree.

Cottbus, November 4th, 2016

Prof. Dr. H. T. Vierhaus
Review report

of the dissertation thesis "Digital Circuits Testing Based on Pattern Overlapping and Broadcasting"

Author: Martin Chloupek
Reviewer: Richard Růžička

Summary and Contribution of the Thesis

In the thesis, author proposes improvement of test application mechanism (compression of test vectors and an on-chip decompressor), previously defined by his predecessors. As the base for the research, the test patterns compression tool COMPAS and on-chip decompressor RESPIN were used. Author of the thesis then developed and implemented a new on-chip decompressor based on utilisation of broadcasting and overlapping techniques to decompress test patterns and a new compression method suitable for the proposed decompressor. Some experimental results, published by the author, are discussed in the thesis and these results prove that the work, done by the author, may contribute to the effort directed towards cheap and reliable testing of large chips.

Up-to-datedness of the Dissertation

The problem, which is addressed by the thesis, is indisputably actual and very important to the contemporary digital circuits design and manufacturing industry. That's why several papers are published each year on this topic. The core of this thesis was published 4 or 5 years ago. Since this time, something new was probably proposed (also by the research group, which the author belongs to). Although the methods and architectures, proposed by the author, are still actual, comparison with recent tools and approaches should enhance the value of experiments published in the thesis.

Formal Structure and Organisation

The thesis is organised clearly, the core, proposed by the author, is distinctly separated from the background and state-of-the-art. The main drawback of the thesis from this point of view is that the text is mainly short. As there are decades of research on that topic behind us, author describes it on 18 pages only. The main contribution together with results of experiments and evaluation – the core of the thesis, author's own research, occupies just 21 pages. Moreover, some of these pages contain just a table or a graph. It is only one chapter, somewhat awkwardly called "Overview." It is a pity that author do not use more graphics, more examples and more explanatory text to elucidate and demonstrate his ideas and experiments. Somewhere, it is to the detriment of intelligibility and a reader must expend higher effort to understand the idea behind the text than is usual for such kind of texts.

Another strange thing in the thesis is utilisation of plural in the text. I understand that the author is a part of the team, the work of the author is a part of a project and there is also the supervisor who brings some ideas to the author, but the main purpose of the thesis is to prove that the author himself is "able to conduct research and achieve scientific results." So in my opinion, the better form (especially in the case of dissertation thesis text) is singular.

Completion of Dissertation Objectives

Objectives of the dissertation thesis are usually not explicitly explained before (like in case of a diploma thesis). I understand as the general objective of the thesis to propose better test access mechanism for complex digital circuits (in terms of test application time), than are contemporary known solutions. In my opinion, submitted thesis fulfils such objective. Author proposes new on-chip
test patterns decompressor together with corresponding test set compression method and scan chain configuration method. The starting point of the research comprised existing solutions – the test patterns compression tool COMPAS and on-chip decompressor RESPIN. Achieved results show that the proposed solutions beat them. So it could be stated that dissertation objectives were achieved.

Assessment of Used Methods
As it was stated above, the part of the thesis, which describes background for the research and state-of-the-art, is somewhat short. But the bibliography of the thesis contains 66 titles, which is enough. Author probably did the literature review and survey in the field of research, but the thesis contains only very brief reflection of the author’s knowledge in the field. Methods, that the author used to reach results published in the thesis are adequate to the dissertation thesis. Maybe algorithms presented in the thesis should be analysed formally in terms of memory and time complexity (e.g. \( \Theta \) function of an input), not only on particular benchmark circuit. But it is not so significant for the assessment.

Evaluation of the Results and Contributions
Proposed broadcast decompressor architecture as well as compression algorithm and proposed scan chain configuration methods were implemented and evaluated using ISCAS benchmark circuits. Results were compared to results achieved by existing test patterns compression tool COMPAS and on-chip decompressor RESPIN. Proposed architecture was also compared in terms of hardware overhead to available commercial tool. Generally, results of experiments for proposed solutions on selected benchmark circuits are better than for existing solutions. There are some minor exceptions and it is a pity that the author does not make any discussion about it. Maybe the proposed method is better for some class of circuits than for another?

Questions for the Defence
Could you explain the importance of regular distribution of structural dependencies between parallel scan chain bits for the proposed compression method?

Overall Evaluation
In spite of above mentioned minor drawbacks of the submitted thesis, results achieved and presented by the author are significant enough in the field of digital circuits testing. Thus, I can say that the author provided the ability to conduct research and achieve scientific results. In accordance with par.47 (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the thesis for the presentation and defence with the aim of receiving the Ph.D. degree.

Brno, December 11th, 2016

Richard Růžička
Review of the PhD dissertation:
“Digital Circuits Testing Based on Pattern Overlapping and Broadcasting”
Submitted by: Martin Chloupek

1. Up-to-datedness of the dissertation.

The dissertation deals with very actual problems associated with the external testing of sequential digital circuits. More specifically, it targets the built-in on-chip scan chain test architectures, which are currently the most prevalent methods for testing such circuits. The test data volume is often very large especially when testing complex sequential circuits. Moreover, the time needed to apply such large test volumes tends to be very long using scan chains. Test compression methods are used to reduce the test data volume that needs to be transferred to the circuit and to shorten the time needed to apply the test.

There is a continuous need for fast test solutions with minimal area overhead in the industry to minimize test cost. The dissertation looks at various test solutions adopted and currently used in industry and proposes a new method. The goal was to improve test time achieved by one of the industrial solutions, namely the COMPAS architecture and the underlying RESPIN architecture, at a reasonable area overhead cost comparable to other state-of-the-art commercial tools.

2. Formal structure and organization of the dissertation.

The formal structure of the dissertation and its organization is standard. It is divided into 4 main sections. Section 1 clearly states the motivation and goals. Section 2 provides a necessary minimal background on related topics such as testing, fault modeling, design for testability and test compression. Some state-of-the-art test solutions adopted by the industry are briefly described using examples, too. Section 3 is the main part of the text and is dedicated to the description and evaluation of the proposed approach, followed by the conclusions and discussion in section 4.

The text in section 3 is often very sparse, making some important concepts harder to understand (e.g., section 3.2.2, section 3.4), and refers the reader to other works published by the author. What is often missing are the examples to better illustrate the proposed concepts (e.g., heuristics H1 – H4 in section 3.2.1). The results provided in figure 3.5 are not discussed at all. The names of some columns in tables 3.1 and 3.3 are not consistent with the names in the text. Some parts of the architecture shown in figure 3.7 are not described in the text. The results in tables 3.5 and 3.6 should have been discussed more precisely, e.g., the total average difference between the proposed architecture and the reference tool should have been stated.

3. Completion of the dissertation objectives.

The author succeeded in proposing a method with reduced test time when compared to the COMPAS and RESPIN architectures and with the area overhead comparable to other state-of-the-art commercial tools, thus completing the objectives of the dissertation. This was proven by performed experiments.

4. Assessment of the methods used in the dissertation.

The evaluations were done solely by experimental measurements with the benchmark digital circuits. Given the nature of the dissertation, this is a very appropriate and common way to evaluate the proposed methods. The obtained results were compared to the results achieved by other methods
with the same set of circuits, proving their validity and usefulness. Therefore, it can be concluded that the proposed methods were evaluated sufficiently.

5. Evaluation of the results and contributions of the dissertation.

The main contribution is the new on-chip test decompression architecture utilizing pattern broadcasting and overlapping. Using the new architecture, a significant test time reduction is possible even for large circuits. However, this comes at a slight test data volume enlargement.

Other contributions include a new scan chain configuration method and a new test compression method, both suitable for the new architecture. Using the new scan chain configuration method, a higher broadcast rates can be achieved than with the random method. The new test compression method did not show any significant improvement over the existing method.

4 of author's other works relevant to the topic of this dissertation were cited in various international forums. This proves that the topic has found acceptance in the scientific community.

6. Remarks, objections, notes, and questions for the defense.

How is the transformation from TVs to TVMs done? A serial approach would take too much time while a parallel approach would require more area. What compromise between the area and time was considered?

Where are the values of TVM weight for each TVM stored?

In section 3.2.1, you mention that the TVM merge process merges TVMs that are “close to each other” and “differ in the minimum no. of 1s”. Is this equivalent to Hamming distance?

The broadcast rate achieved by the heuristic H4 in Table 3.2 for the circuit b11 is lower than for the random approach (43 % and 45 %, respectively). This should not be the case since heuristics are proposed to improve the random approach. Could you explain this anomaly?

Are there any specific requirements on how to represent the logical values ‘0’, ‘1’ and ‘x’ in TVs from ATPG that are inputs to the proposed compression algorithm? One bit is clearly not enough to represent 3 possible values.

In section 3.3.0.1, you state that the future research should focus on finding different method than test pattern compaction to cover other faults not covered by the overlapping. Can you suggest what kind of methods would be a good alternative?

Could you provide more details about the reference tool that was used to compare the area overhead of the proposed architecture?

7. The overall evaluation of the dissertation.

The dissertation contains numerous typos and spelling errors. There are some stylistic errors too which make some parts of the text slightly harder to understand.

Despite numerous formal flaws in the text and despite often being sparse when describing proposed concepts, instead referring the reader to other works published by the author, I think the obtained results are very interesting and definitely contribute to the existing knowledge in the area of sequential circuit testing. Using the proposed architecture, the test time of even large sequential circuits can be greatly reduced at the cost of slight test data volume increase which can be considered as an acceptable tradeoff. This has the potential to help reduce test costs and time-to-market for industry.
The author of the dissertation proved the ability to conduct research and achieve scientific results. In accordance with par. 47, letter (4) of the Law Nr. 111/1998 (The Higher Education Act) I do recommend the dissertation for the presentation and defense with the aim of receiving the Ph.D. degree.

Bratislava, December 12, 2016

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